WHAT IS CLAIMED IS:

1. A computer implemented method of approximating a gray scale tone with a more limited range image producer, comprising the steps of:

associating one of a plurality of tone curves with each pixel of a screening matrix;

generating polynomial coefficients of a curve approximating each of said plurality of tone curves;

storing said polynomial coefficients approximating each of said plurality of tone curves in a look-up table;

mapping each pixel of an image to a corresponding pixel of said screening matrix;

for each pixel of said image

recalling said polynomial coefficients approximating said tone curve associated with said pixel of said screening matrix mapped to said pixel, and

computing a pixel output value from a pixel input value of said pixel and said recalled polynomial coefficients.

2. The computer implemented method of claim 1, wherein:

said polynomial is a third degree polynomial of the form

$$y = ((a * x + b) * x + c) * x$$

where: y is the pixel output value to be computer; a is a first coefficient; b is a second coefficient; c is a third coefficient; and x is the pixel input value.

3. The computer implemented method of claim 2, wherein:

said step of computing a pixel output value includes

multiplying said pixel input value by said first coefficient producing a first intermediate value,

adding said second coefficient to said first intermediate value producing a second intermediate value,

multiplying said second intermediate value by said pixel input value producing a third intermediate value,

adding said third coefficient to said third intermediate value producing a fourth intermediate value, and

multiplying said fourth intermediate value by said pixel input value producing said pixel output value.

4. The computer implemented method of claim 2, wherein:

said step of computing a pixel output value computes a first pixel output value and a second pixel output value by sequentially

(1) multiplying a first pixel input value by a first coefficient corresponding to said first pixel producing a first intermediate value,

(2) simultaneously multiplying a second pixel input value by a first coefficient corresponding to said second pixel producing a second intermediate value, and adding a second coefficient corresponding to said first pixel to said first intermediate value producing a third intermediate value,

(3) simultaneously multiplying said third intermediate value by said first pixel input value producing a fourth intermediate value, and adding a

second coefficient corresponding to said second pixel to said second intermediate value producing a fifth intermediate value,

(4) simultaneously multiplying said fifth intermediate value by said second pixel input value producing a sixth intermediate value, and adding said third coefficient corresponding to said first pixel to said fourth intermediate value producing a seventh intermediate value,

(5) simultaneously multiplying said seventh intermediate value by said first pixel input value producing said first pixel output value, and adding said third coefficient corresponding to said second pixel to said sixth intermediate value producing an eighth intermediate value, and

(6) multiplying said eighth intermediate value by said second pixel input value producing said second pixel output value.

5. The computer implemented method of claim 4, wherein:

said pixel input values are represented in a fixed point representation of 8 bits including zero integer bits and eight fractional bits;

said first, second and third coefficients corresponding to each tone curve are represented in a fixed point representation of 16 bits including four integer bits and twelve fractional bits;

said step of adding said second coefficient corresponding to said first pixel to said first intermediate value producing

a third intermediate value includes right shifting said first intermediate value 8 bits prior to addition;

said step of adding said second coefficient corresponding to said second pixel to said second intermediate value producing a fifth intermediate value includes right shifting said second intermediate value by 8 bits prior to addition;

said step of adding said third coefficient corresponding to said first pixel to said fourth intermediate value producing a seventh intermediate value includes right shifting said fourth intermediate value by 8 bits prior to addition; and

said step of adding said third coefficient corresponding to said second pixel to said sixth intermediate value producing an eighth intermediate value includes right shifting said sixth intermediate value by 8 bits prior to addition.

6. A printer comprising:

a transceiver adapted for bidirectional communication with a communications channel;

a memory;

a print engine adapted for placing color dots on a printed page according to received image data and control signals; and

a programmable data processor connected to said transceiver, said memory and said print engine, said programmable data processor programmed to:

receive print data corresponding to pages to be printed from the communications channel via said transceiver;

convert said print data into image data and control signals for supply to said print engine for printing a corresponding page, said conversion including approximating a gray scale tone with a more limited range print engine by

storing polynomial coefficients approximating each of a plurality of tone curves in a look-up table,

mapping each pixel of an image to a corresponding pixel of a screening matrix;

for each pixel of said image

recalling a corresponding set of polynomial coefficients approximating a tone curve associated with said pixel of said screening matrix mapped to said pixel, and

computing a pixel output value from a pixel input value of said pixel and said recalled polynomial coefficients.

7. The printer of claim 6, wherein:

said programmable data processor including a hardware multiplier and an arithmetic logic unit, said programmable data processor being further programmed to compute said pixel output value by

multiplying said pixel input value by said first coefficient in said hardware multiplier producing a first intermediate value,

adding said second coefficient to said first intermediate value in said arithmetic logic unit producing a second intermediate value,

multiplying said second intermediate value by said pixel input value in said hardware multiplier producing a third intermediate value,

adding said third coefficient to said third intermediate value in said arithmetic logic unit producing a fourth intermediate value, and

multiplying said fourth intermediate value by said pixel input value in said hardware multiplier producing said pixel output value.

8. The printer of claim 6, wherein:

said programmable data processor including a hardware multiplier and an arithmetic logic unit, said programmable data processor being further programmed to compute said pixel output value by

(1) multiplying a first pixel input value by a first coefficient corresponding to said first pixel in said hardware multiplier producing a first intermediate value,

(2) simultaneously multiplying a second pixel input value by a first coefficient corresponding to said second pixel in said hardware multiplier producing a second intermediate value, and adding a second coefficient corresponding to said first pixel to said first intermediate value in said arithmetic logic unit producing a third intermediate value,

(3) simultaneously multiplying said third intermediate value by said first pixel input value in said hardware multiplier producing a fourth intermediate value, and adding a second coefficient corresponding to

said second pixel to said second intermediate value in said arithmetic logic unit producing a fifth intermediate value,

(4) simultaneously multiplying said fifth intermediate value by said second pixel input value in said hardware multiplier producing a sixth intermediate value, and adding said third coefficient corresponding to said first pixel to said fourth intermediate value in said arithmetic logic unit producing a seventh intermediate value,

(5) simultaneously multiplying said seventh intermediate value by said first pixel input value in said hardware multiplier producing said first pixel output value, and adding said third coefficient corresponding to said second pixel to said sixth intermediate value in said arithmetic logic unit producing an eighth intermediate value, and

(6) multiplying said eighth intermediate value by said second pixel input value in said hardware multiplier producing said second pixel output value.

9. The printer of claim 8, wherein:

said programmable data processor further including a shifter at one input to said arithmetic logic unit, said programmable data processor being further programmed to compute said pixel output value by

right shifting said first intermediate value 8 bits prior to addition;

right shifting said second intermediate value by 8 bits prior to addition;

right shifting said fourth intermediate value by 8 bits prior to addition; and

right shifting said sixth intermediate value by 8 bits prior to addition.